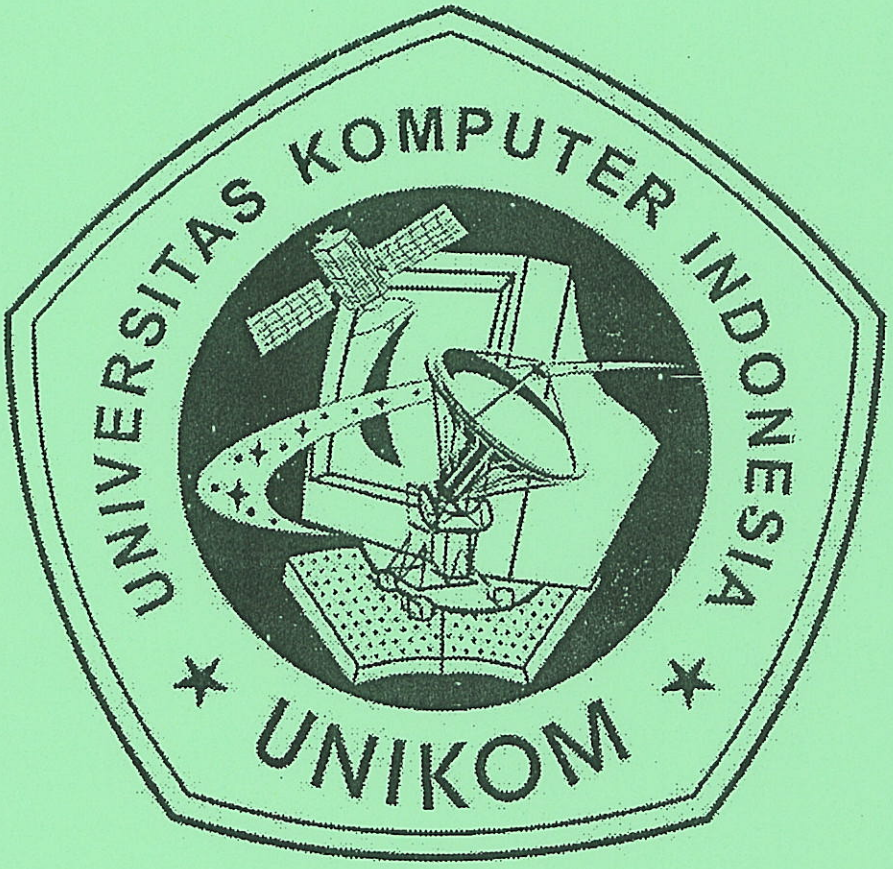
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Joglyanto H.M Pengenalan KOMPUTER (Dasar Ilmu Komputer, Pemrograman, Sistem Informasi dan Integelensi Buatan). Penerbit ANDI OFFSET Yogyakarta.


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FAIRCHILD
SEMICONDUCTOR™

July 1998

NM27C210
1,048,576-Bit (64K x 16) High Performance CMOS EPROM

General Description

The NM27C210 is a high performance Electrically Programmable UV erasable ROM (EPROM). It contains 1,048,576 bits configured as 64K x 16 bit. It is offered in both erasable versions for prototyping and early production applications as well as non-erasable, plastic packaged versions that are ideal for high volume and automated assembly applications.

The NM27C210 operates from a single 5 volt ±10% supply in the read mode.

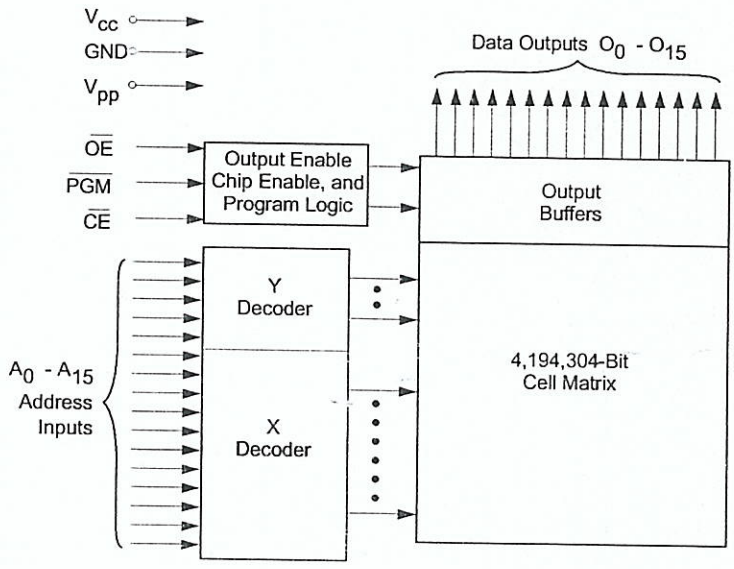
The NM27C210 is offered in both DIP and surface mount packages. The DIP package is a 40-pin dual-in-line ceramic with a quartz window to allow erasing. The surface mount package is a 44-pin PLCC that is offered in OTP.

This EPROM is manufactured using Fairchild's proprietary AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

Features

- High performance CMOS
  - —90 ns access time
- Fast turn-off for microprocessor compatibility
- Simplified upgrade path
  - —V_{PP} and PGM are "Don't Care" during normal read operation
- Compatible with 27210 and 27C210 EPROMs
- Manufacturer's identification code
- Fast programming
- JEDEC standard pin configuration
  - —40-pin CDIP package
  - —40-pin PDIP package
  - —44-pin PLCC package

Block Diagram



DS011093-1

AMG™ is a trademark of WSI, Inc.

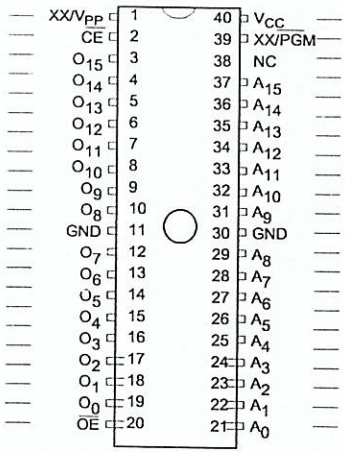
© 1998 Fairchild Semiconductor Corporation

Connection Diagrams

DIP PIN CONFIGURATIONS

27C280	27C240	27C220
A_{18}	XXV_{PP}	XXV_{PP}
$\overline{CE}/PGM$	$\overline{CE}/PGM$	$\overline{CE}$
O_{15}	O_{15}	O_{15}
O_{14}	O_{14}	O_{14}
O_{13}	O_{13}	O_{13}
O_{12}	O_{12}	O_{12}
O_{11}	O_{11}	O_{11}
O_{10}	O_{10}	O_{10}
O_9	O_9	O_9
O_8	O_8	O_8
GND	GND	GND
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3
O_2	O_2	O_2
O_1	O_1	O_1
O_0	O_0	O_0
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$

DIP
NM27C210



27C220	27C240	27C280
V_{CC}	V_{CC}	V_{CC}
PGM	A_{17}	A_{17}
A_{16}	A_{16}	A_{16}
A_{15}	A_{15}	A_{15}
A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}
A_{12}	A_{12}	A_{12}
A_{11}	A_{11}	A_{11}
A_{10}	A_{10}	A_{10}
A_9	A_9	A_9
GND	GND	GND
A_8	A_8	A_8
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C210 pins.

DS011093-7

Commercial Temperature Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 Q, V, N 90	90
NM27C210 Q, V, N 120	120
NM27C210 Q, V, N 150	150

Industrial Temperature Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 QE, VE, NE 120	120
NM27C210 QE, VE, NE 150	150

Package Types: NM27C210 Q, V, N XXX

Q = Quartz-Windowed Ceramic DIP package

N = Plastic DIP package

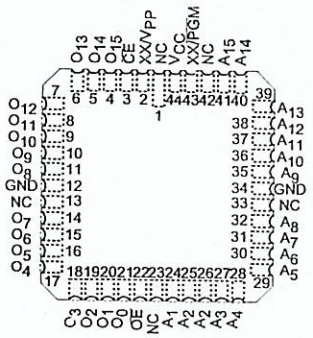
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
PGM	Program
XX	Don't Care (During Read)
NC	No Connect

PLCC Pin Configuration



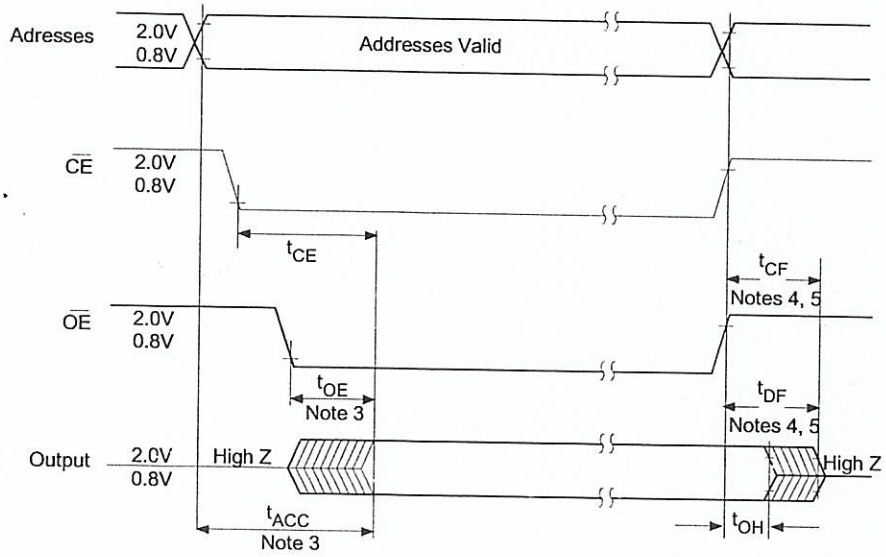
Top View

DS011093-3

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 6) , (Note 7) , (Note 9)



DS011093-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

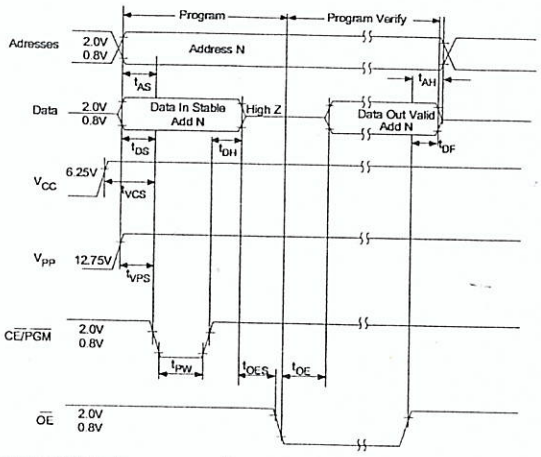
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Note 11), (Note 12), (Note 13), (Note 14), and (Note 15)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	CE Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from OE	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 13)



DS011093-5

Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

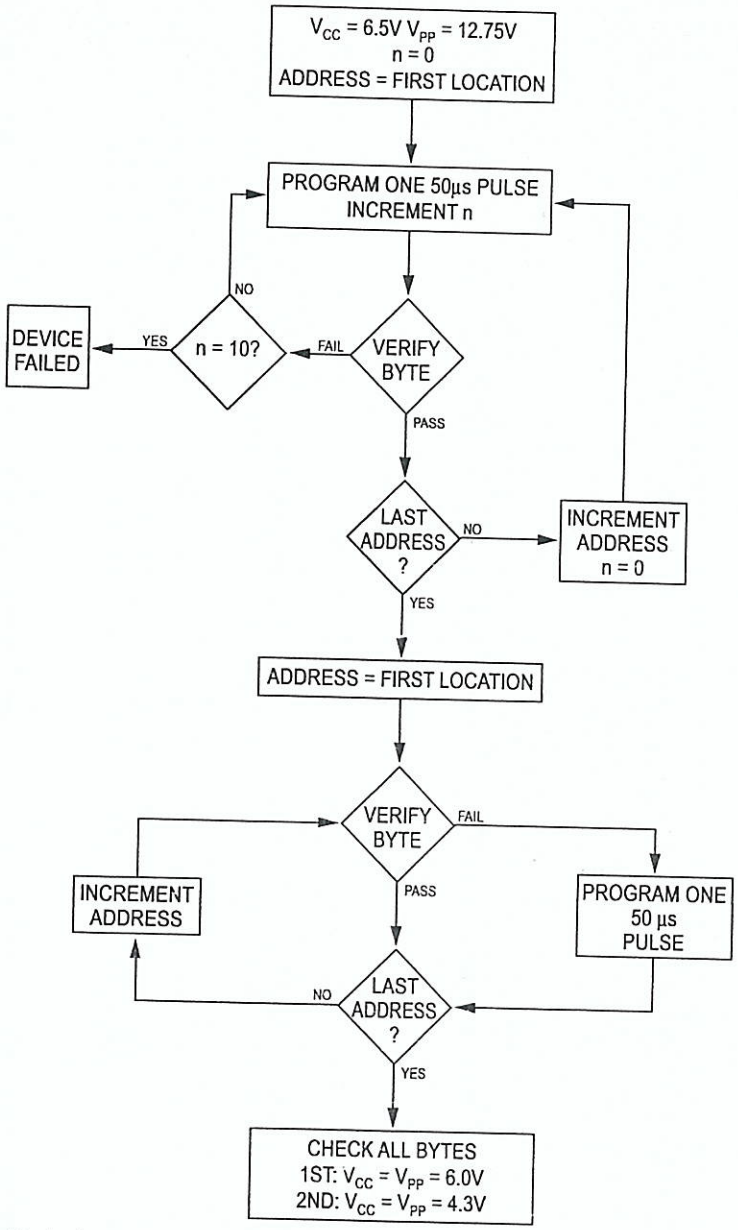
Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: Programming and program verify are tested with the turbo Program Algorithm, at typical power supply voltages and timings.

Note 15: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Turbo Programming Algorithm Flow Chart



Note: The standard National Semiconductor algorithm may also be used but it will have longer programming time.

DS011093-6

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 200 mW to 0.5 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time).

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for the NM27C210 is "8FD6", where "8F" designates that it is made by Fairchild Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1 – A8, A10 – A15, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held

Functional Description (Continued)

at V_{IH} for the device code. The code is read on the lower eight data pins, O0 –07 . Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27C210 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

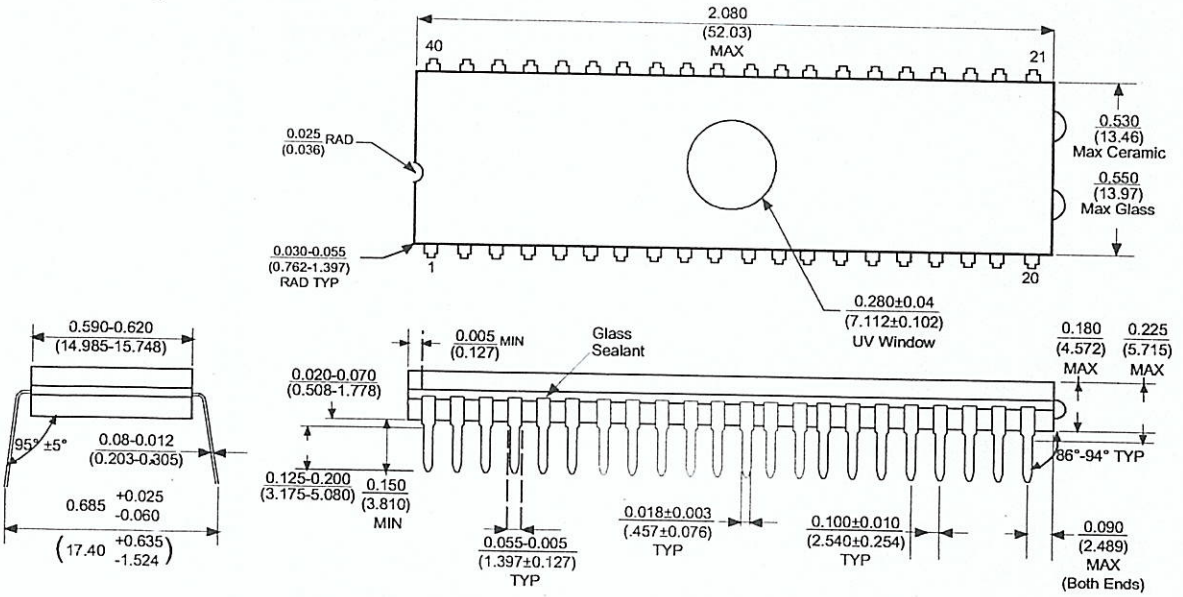
Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 16)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 16: X can be V_{IL} or V_{IH}.

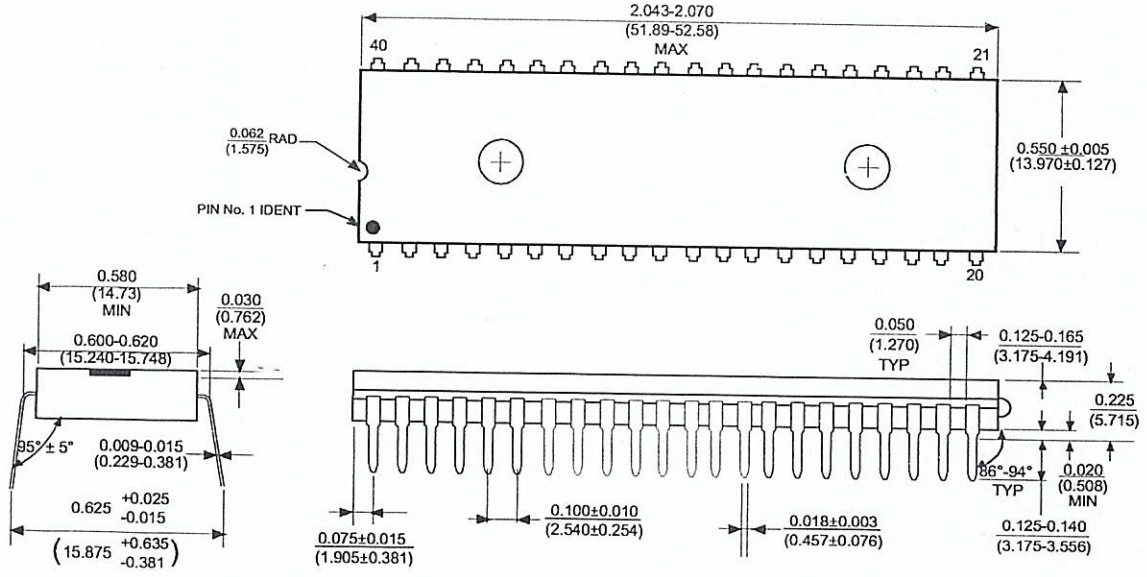
TABLE 2. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O7 (12)	O6 (13)	O5 (14)	O4 (15)	O3 (16)	O2 (17)	O1 (18)	O0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

Physical Dimensions inches (millimeters) unless otherwise noted

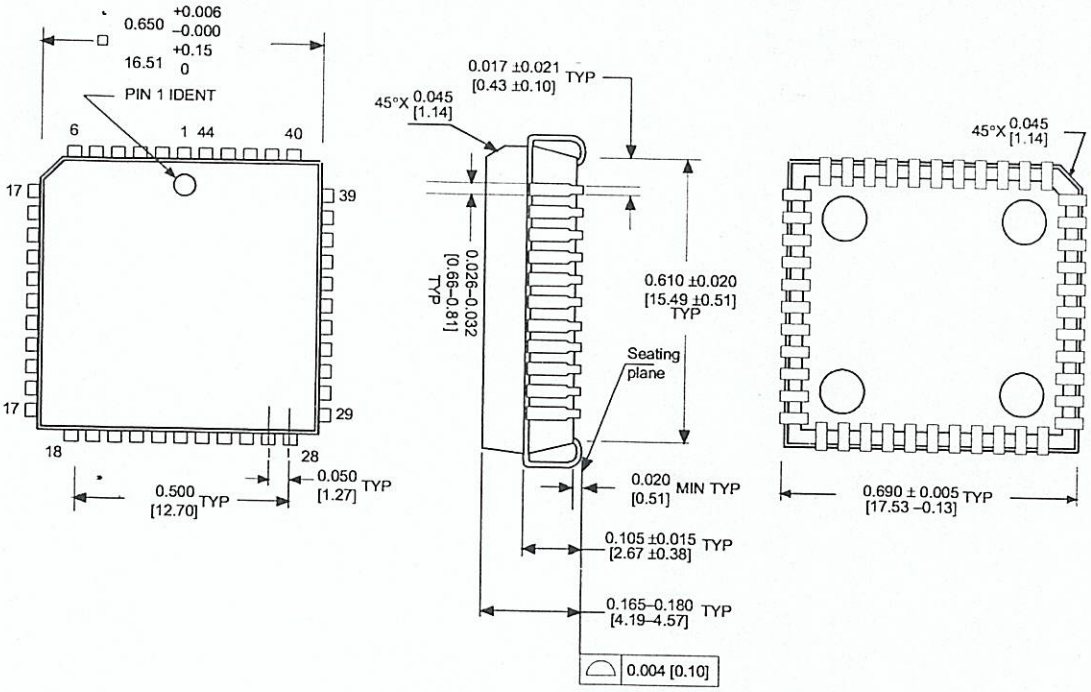


40-Lead EPROM Ceramic Dual-In-Line Package (Q)
Order Number NM27C210QXXX
Package Number J40BQ



40-Lead Molded Dual-In-Line Package (N)
Order Number NM27C210NXXX
Package Number N40A

Physical Dimensions inches (millimeters) unless otherwise noted



44-Lead Plastic Chip Carrier (V)
Order Number NM27C210VXXX
Package Number V44A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Alamat Perusahaan & Telepon : JL. IR. H. JUANDA

Waktu Kerja Praktek : 1 - SEPTEMBER

Nama Pejabat Penilai : IR. ISKANDAR YUSUF, MSC

Jabatan :

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1	Disiplin Dalam Kerja	86	A
2	Kemampuan menyelesaikan Tugas	80	A
3	Prestasi Kerja	81	A
4	Inisiatif	80	A
5	Kepribadian	80	A

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materi KP yg UNIKOM masih perlu kita lebih lanjut waktu pelaksanaan yg cukup lama.

NILAI	INDEKS	KETERANGAN
80 < NA < 100	A	Sangat Baik
70 < NA < 79	B	Baik
55 < NA < 69	C	Cukup
41 < NA < 54	D	Kurang
0 < NA < 40	E	Buruk

BANDUNG, 10 MARET 2007

Mengetahui,

Koordinator Kerja Praktek

Yeffry Handoko Putra, ST., MT

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